WHAT IS CLAIMED IS:

1. A method comprising:

receiving a serial stream of data bits;

deserializing the serial stream of data bits into parallel bits;

inputting the parallel bits into a content addressable memory and a first register;

inputting an output of the first register into a second register;

inputting outputs of the first and second registers to the content addressable memory;

providing the parallel bits in a plurality of parallel bit output formats; and

selecting one of the parallel bit output formats to output based on match flag outputs from the content addressable memory, wherein the match flag outputs are generated in response to the inputs to the content addressable memory.

2. The method of claim 1 wherein the plurality of parallel bit output formats are input to a plurality of tristate driver circuits, and selecting one of the parallel bit output formats to output comprises:

enabling one of the tristate driver circuits to output the parallel bit output format associated with that tristate driver circuits to an output bus, and disabling other ones of the tristate driver circuits coupled to the output bus.

3. The method of claim 1 wherein there are eight parallel bits.

4. The method of claim 1 wherein the first and second registers are two stages of a shift register.

5. The method of claim 1 wherein a depth of the content addressable memory comprises at least one row for each of the parallel bits.

6. The method of claim 1 wherein the inputs to the content addressable memory are provided by way of parallel transfer.

7. The method of claim 6 wherein a width of the parallel bits inputting the content addressable memory is at least a number of parallel bits output from the deserializer plus a length of a pattern to be detected using the content addressable memory minus 1.

8. A circuit comprising:

a deserializer circuit coupled to receive serial data input and outputting a first parallel data of output;

a shift register coupled to the first parallel data output; and

a content addressable memory, coupled to the shift register to receive the first parallel data output in parallel.

9. The circuit of claim 8 further comprising:

a plurality of parallel data output formats based on the first parallel data output; and

a plurality of tristate buffer circuits, one coupled to each of the parallel data output formats.

10. The circuit of claim 9 further comprising:

a control logic block, coupled to a match signal from the content addressable memory, generating a plurality of select signals, one coupled to each of the tristate buffer circuits.

11. The circuit of claim 10 wherein based on the match signal, the control logic block generates select signals to enable one of the tristate buffers and disable others of the tristate buffers.

12. The circuit of claim 10 wherein the control logic block comprises a state machine.

13. The circuit of claim 9 wherein there is one parallel data output format for each bit of the first parallel data output minus 1.

14. The circuit of claim 8 wherein the shift register is divided into three portions, the first portion of the shift register is coupled to the deserializer, the second portion of

the shift register is coupled to the first portion through a first multiplexer, and the third portion of the shift register is coupled to the second portion through a second multiplexer.

15. The circuit of claim 14 wherein the third position of the shift register is coupled to the first portion of the shift register through the second multiplexer.

16. The circuit of claim 14 wherein the second position of the shift register is coupled to the deserializer through the first multiplexer.

17. The circuit of claim 8 wherein each row in the content addressable memory comprises a data pattern to be detected in the serial data input.

18. The circuit of claim 8 wherein the content addressable memory has a number of rows equal to or greater than a number of bits of the first parallel data output.

19. The circuit of claim 8 wherein the content addressable memory comprises a bit pattern comprising "1111," "0110," "0010," and "1000" in at least a number of rows that is equal to a number of bits of the first parallel data output.

20. The circuit of claim 8 wherein the first parallel data output is 8, 10, 16, or 20 bits wide.

21. A programmable logic integrated circuit comprising the circuit of claim 8.

22. The circuit of claim 8 further comprising:

a plurality of parallel data output formats based on the first parallel data output; and

a selector circuit, coupled to each of the parallel data output formats and the first parallel data output, outputting one of the parallel data output formats as a second parallel data output based on an output from the content addressable memory.

23. The circuit of claim 8 wherein the first parallel data output comprises 8 bits in a format bit 0, bit 1, bit 2, bit 3, bit 4, bit 5, bit 6, and bit 7, and the circuit further comprises:

a first parallel data output format comprising bit 1, bit 2, bit 3, bit 4, bit 5, bit 6, bit 7, and bit 0;

a second parallel data output format comprising bit 2, bit 3, bit 4, bit 5, bit 6, bit 7, bit 0, and bit 1; and

a third parallel data output format comprising bit 3, bit 4, bit 5, bit 6, bit 7, bit 0, bit 1 and bit 2;

a fourth parallel data output format comprising bit 4, bit 5, bit 6, bit 7, bit 0, bit 1, bit 2, and bit 3;

a fifth parallel data output format comprising bit 5, bit 6, bit 7, bit 0, bit 1, bit 2, bit 3, and bit 4;

a sixth parallel data output format comprising bit 6, bit 7, bit 0, bit 1, bit 2, bit 3, bit 4, and bit 5; and

a seventh parallel data output format comprising bit 7, bit 0, bit 1, bit 2, bit 3, bit 4, bit 5, and bit 6.